

Docket No.: 57454-963

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
	:	
Hiroshi Maeda, et al.	:	Confirmation Number: To be assigned
	:	
Serial No.: Divisional of	:	Group Art Unit: To be assigned
Application No. 09/903,735	:	
	:	
Filed: August 05, 2003	:	Examiner: To be assigned
	:	
For: SEMICONDUCTOR DEVICE WITH CAPACITOR ELECTRODES AND METHOD OF		
MANUFACTURING THEREOF		

INFORMATION DISCLOSURE STATEMENT

Mail Stop NEW APPLICATIONS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached form PTO-1449. It is respectfully requested that the references be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

The references were cited by or submitted to the U.S. Patent and Trademark Office in parent application Serial No. 09/903,735 , filed July 13, 2001 , which is relied upon for an

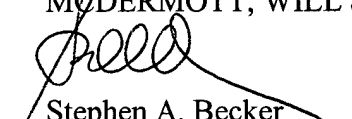
Serial No.: Divisional of
Application No. 09/903,735

earlier filing date under 35 USC 120. Thus, copies of these references are not attached. 37 CFR
1.98(d).

Please charge any shortage in fees due in connection with the filing of this paper, including
extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit
account.

Respectfully submitted,

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INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)			ATTY. DOCKET NO. 57454-963		SERIAL NO. Divisional of Serial No. 09/903,735	
			APPLICANT Hiroshi MAEDA, ET AL.			
			FILING DATE August 5, 2003		GROUP To be assigned	
U.S. PATENT DOCUMENTS						
EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	6,424,011	07/2002	Assaderaghi et al	257	350	
	6,255,151	07/2001	Fukuda et al	257	296	
FOREIGN PATENT DOCUMENTS						
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation
						Yes No
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)						
	M. Igarashi, A. Harada, H. Amishiro, H. Kawashima, N. Morimoto, Y. Kusumi, T. Saito, A. Ohsaki, T. Mori, T. Fukada, Y. Toyoda, K. Higashitani, and H. Arima, "The Best Combination Of Aluminum and Copper Interconnects For a High Performance 0.18 μ m CMOS Logic Device," IEDM98, 1998, PP. 829-832.					
	J. Heidenreich, D. Edelstein, R. Goldblatt, W. Cote, C. Uzoh, N. Lustig, T. McDevitt, A. Stamper, A. Simon, J. Dukovic, R. Wachnik, H. Rathore, S. Luce, and J. Slattery, "Copper Dual Damascene Wiring for Sub-0.25 μ m CMOS Technology," PP. 13-15.					
EXAMINER			DATE CONSIDERED			

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.